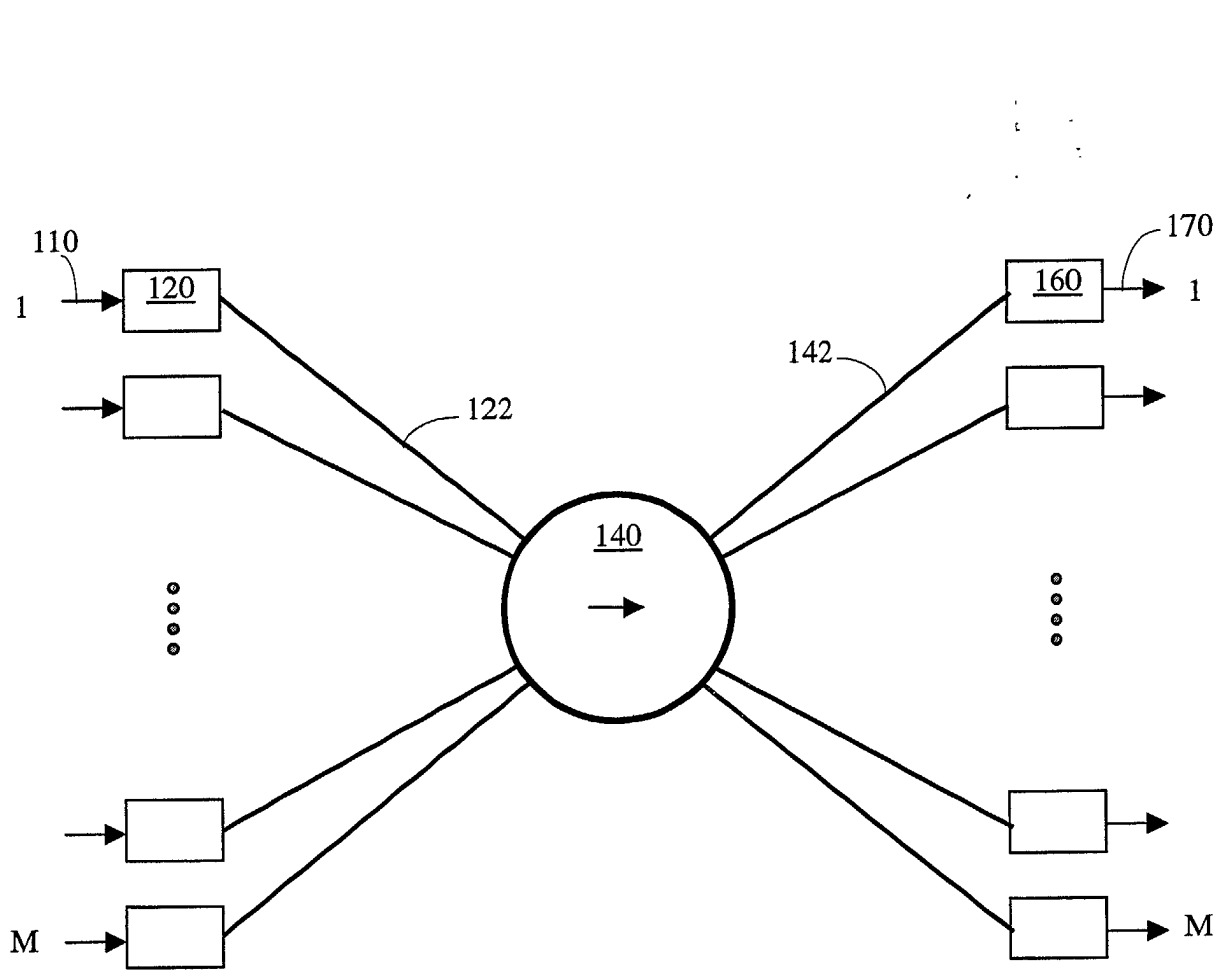


Fig. 1

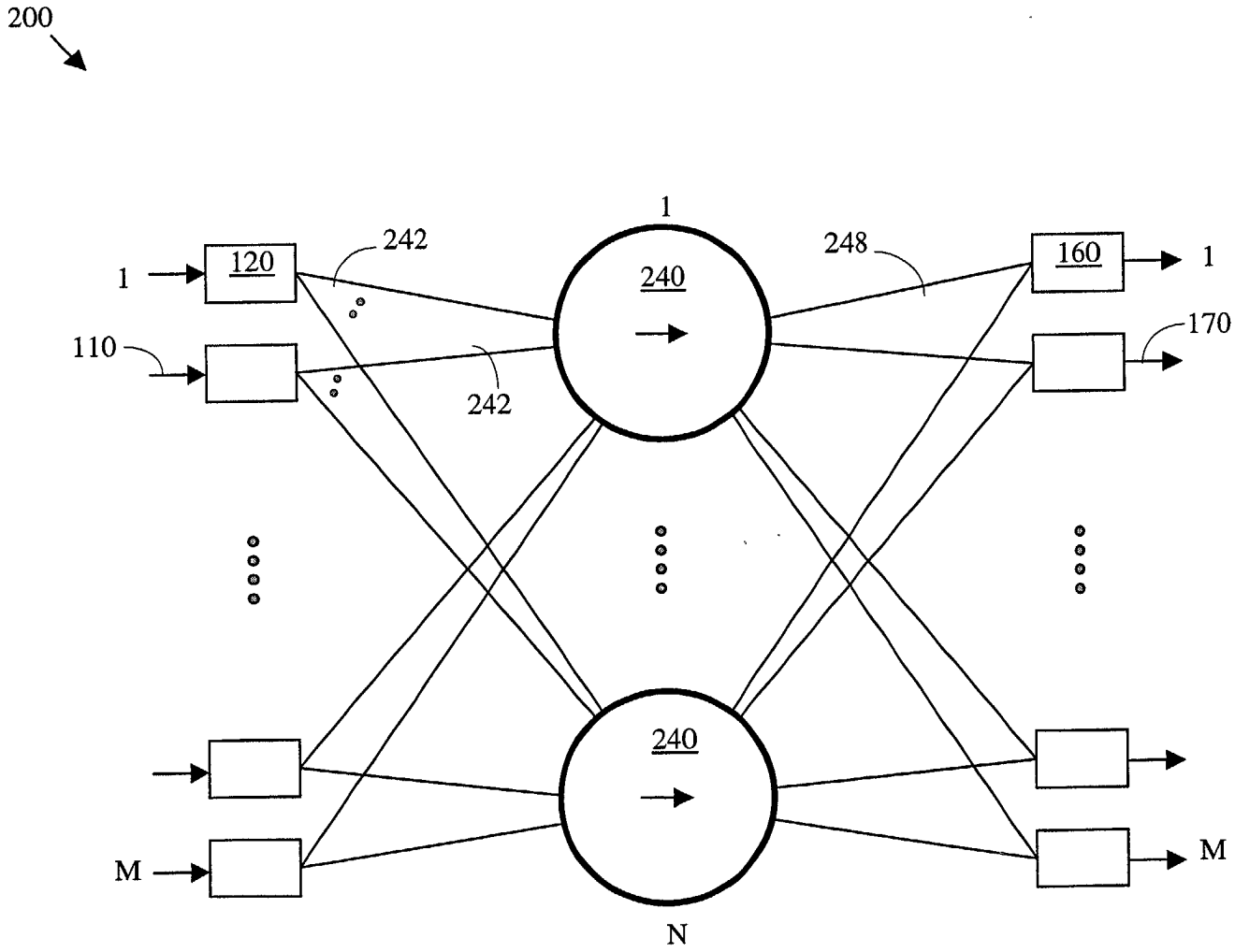


Fig. 2

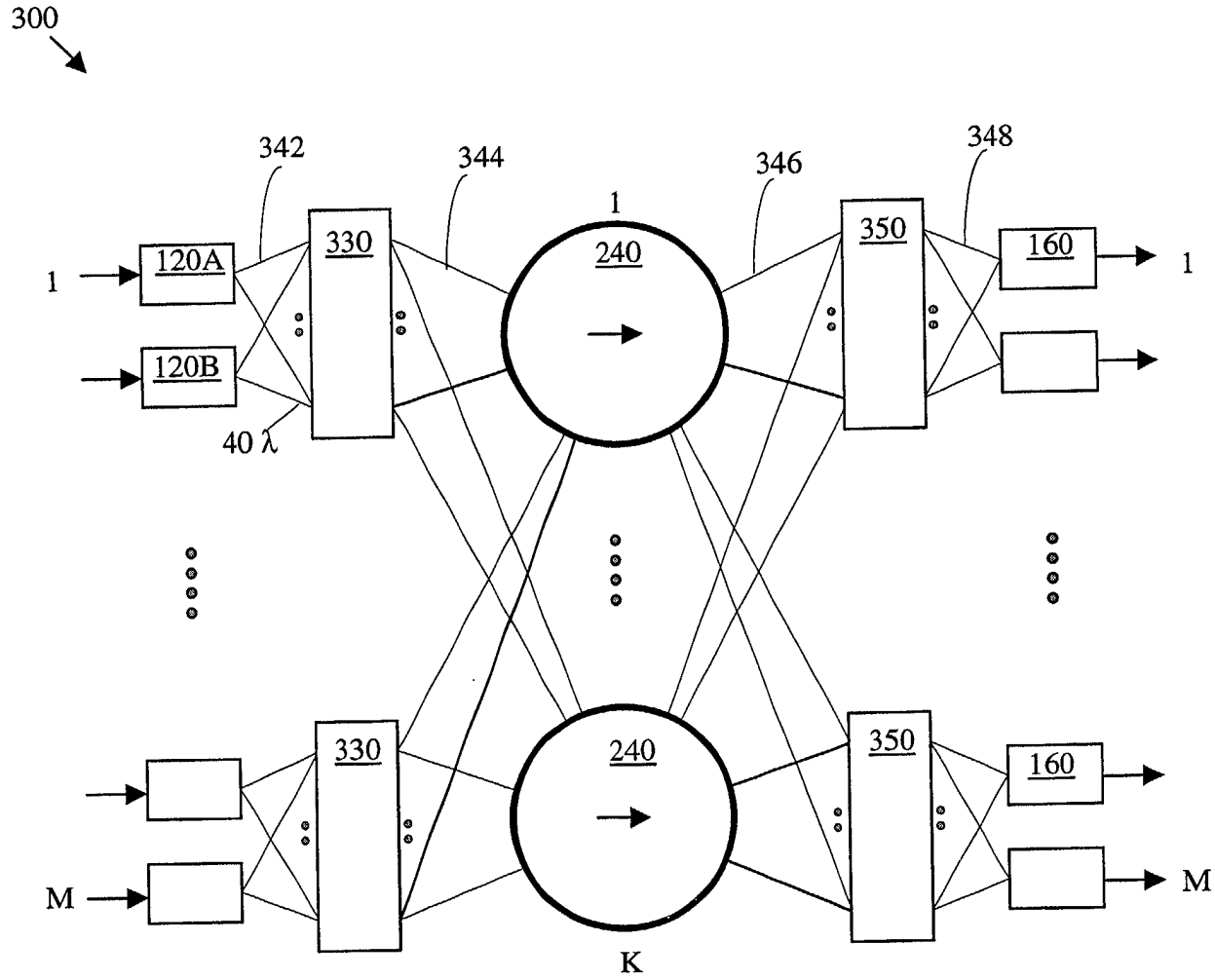

300
342
344
346
348
1
120A
120B
330
240
350
160
1
40 λ
330
240
350
160
M
M
K

Fig. 3

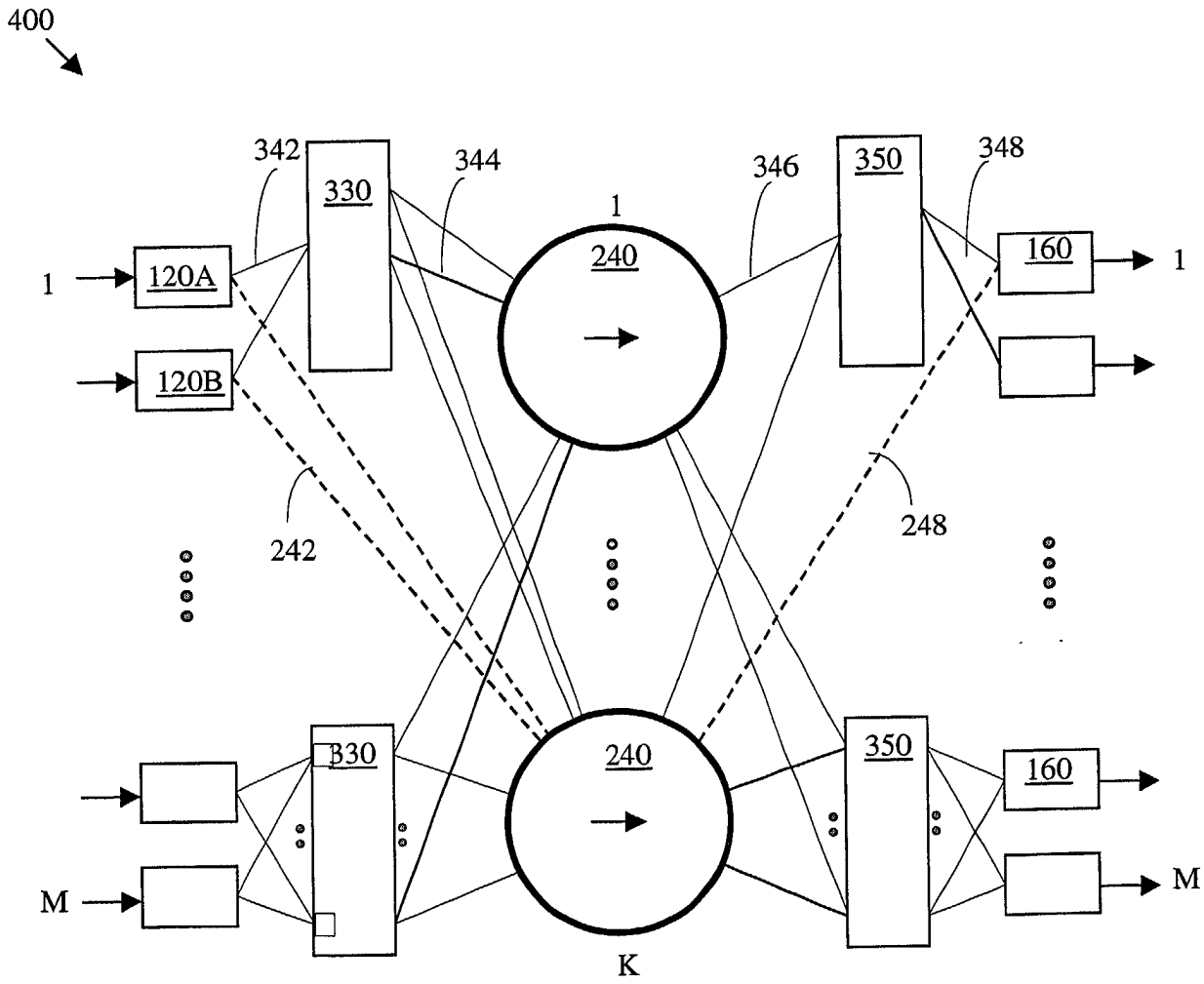
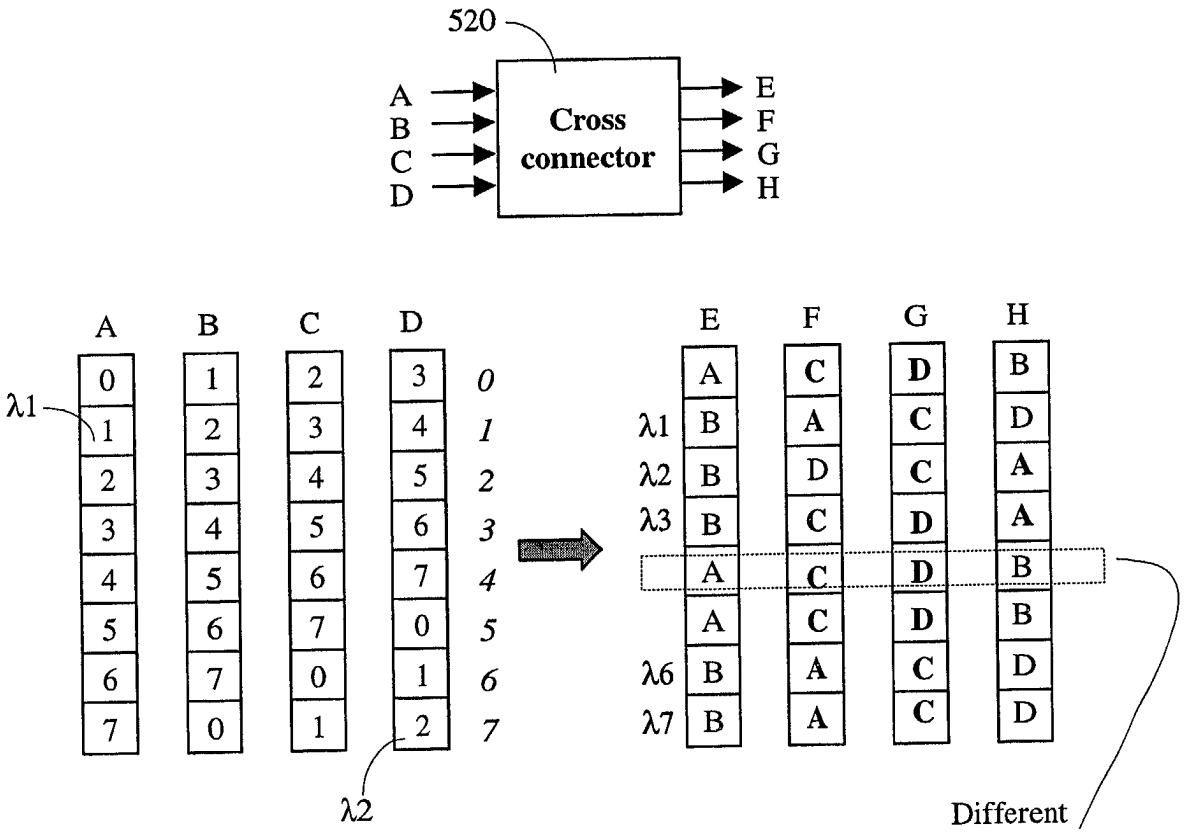

400
342
330
344
1
240
346
350
348
160
1
1
120A
120B
242
248
330
240
350
160
M
M
K

Fig. 4



Example: Virtual link {λ1, λ2, λ3, λ6, λ7}

Fig. 5

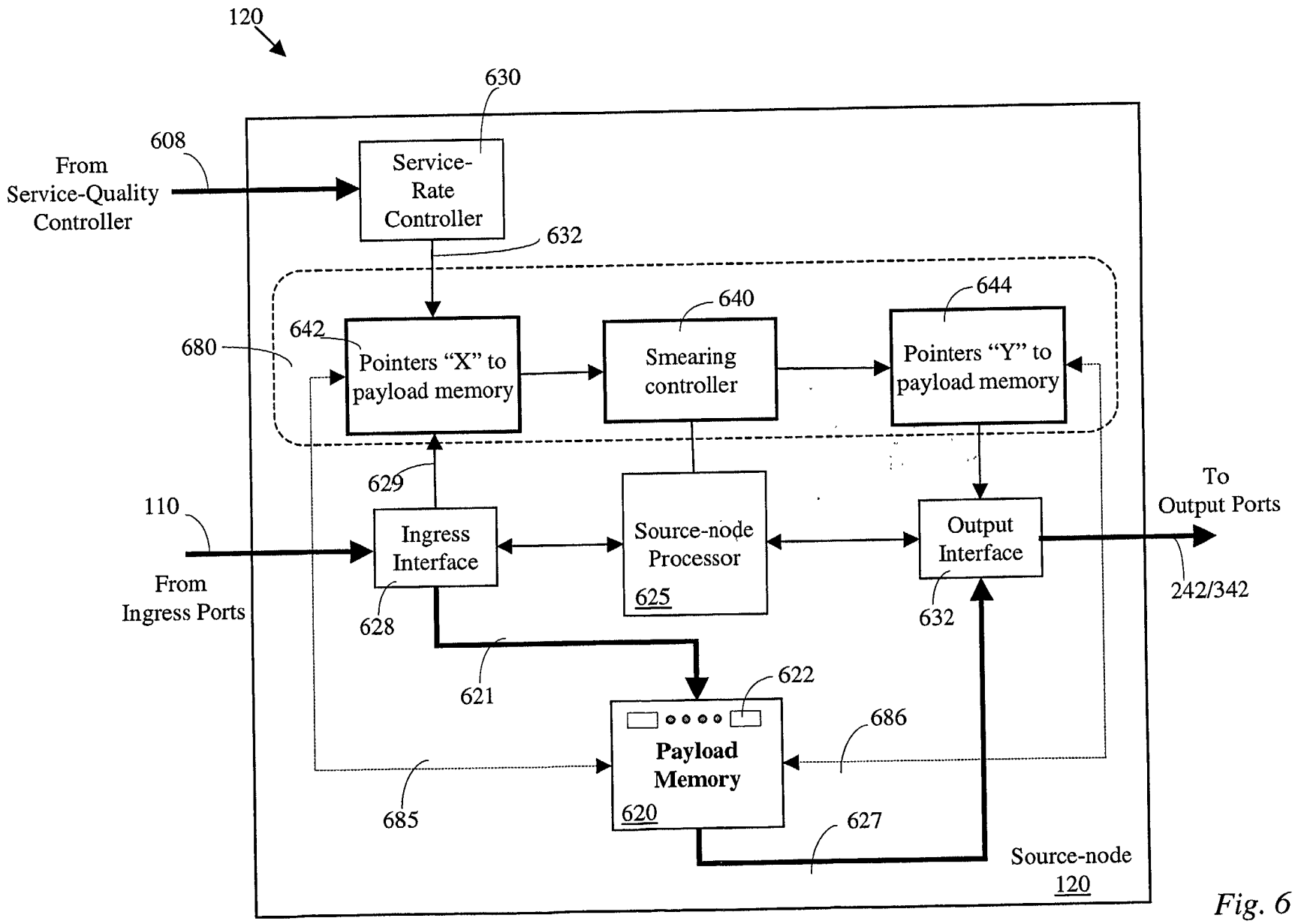

120
630
608
From
Service-Quality
Controller
Service-
Rate
Controller
632
642
680
Pointers "X" to
payload memory
640
Smearing
controller
644
Pointers "Y" to
payload memory
629
110
From
Ingress Ports
Ingress
Interface
628
Source-node
Processor
625
Output
Interface
632
To
Output Ports
242/342
621
622
686
Payload
Memory
620
685
627
Source-node
120

Fig. 6

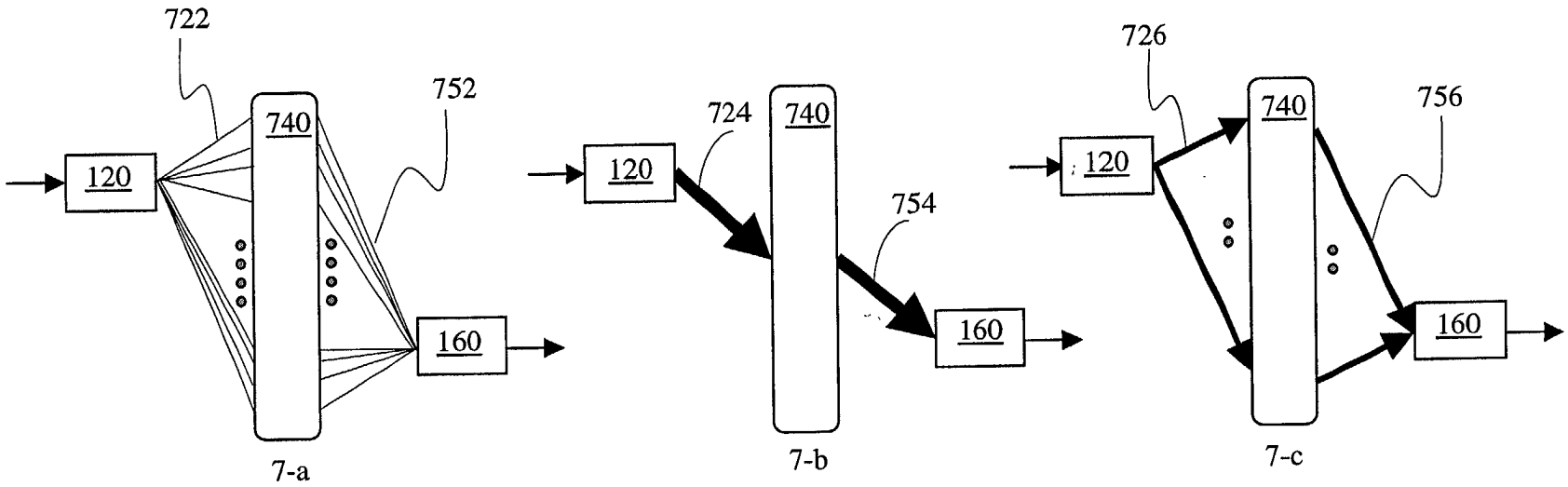

722
752
740
120
160
7-a
724
740
754
120
160
7-b
726
740
756
120
160
7-c

Fig. 7

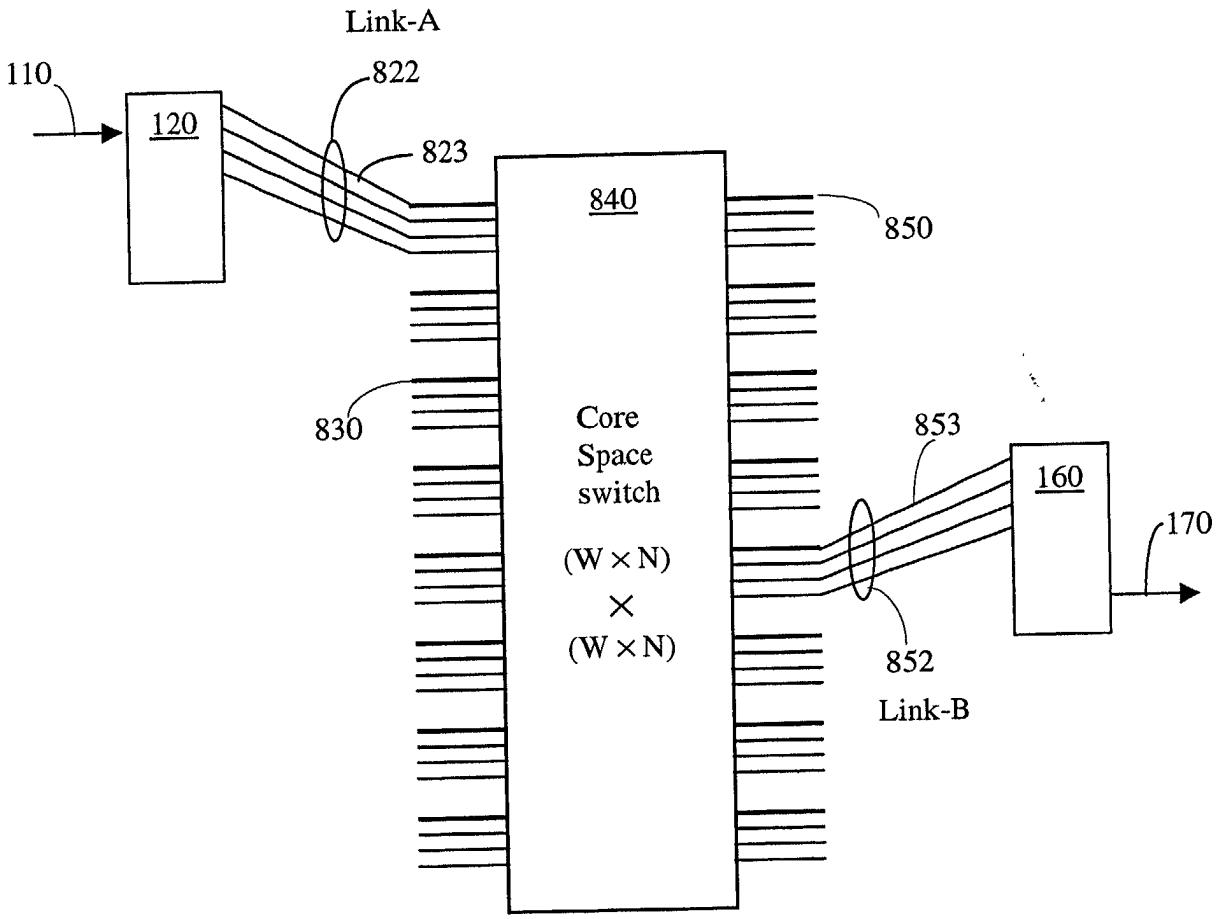

Link-A
110
120
822
823
840
850
830
Core
Space
switch
(W × N)
×
(W × N)
853
160
170
852
Link-B

Fig. 8

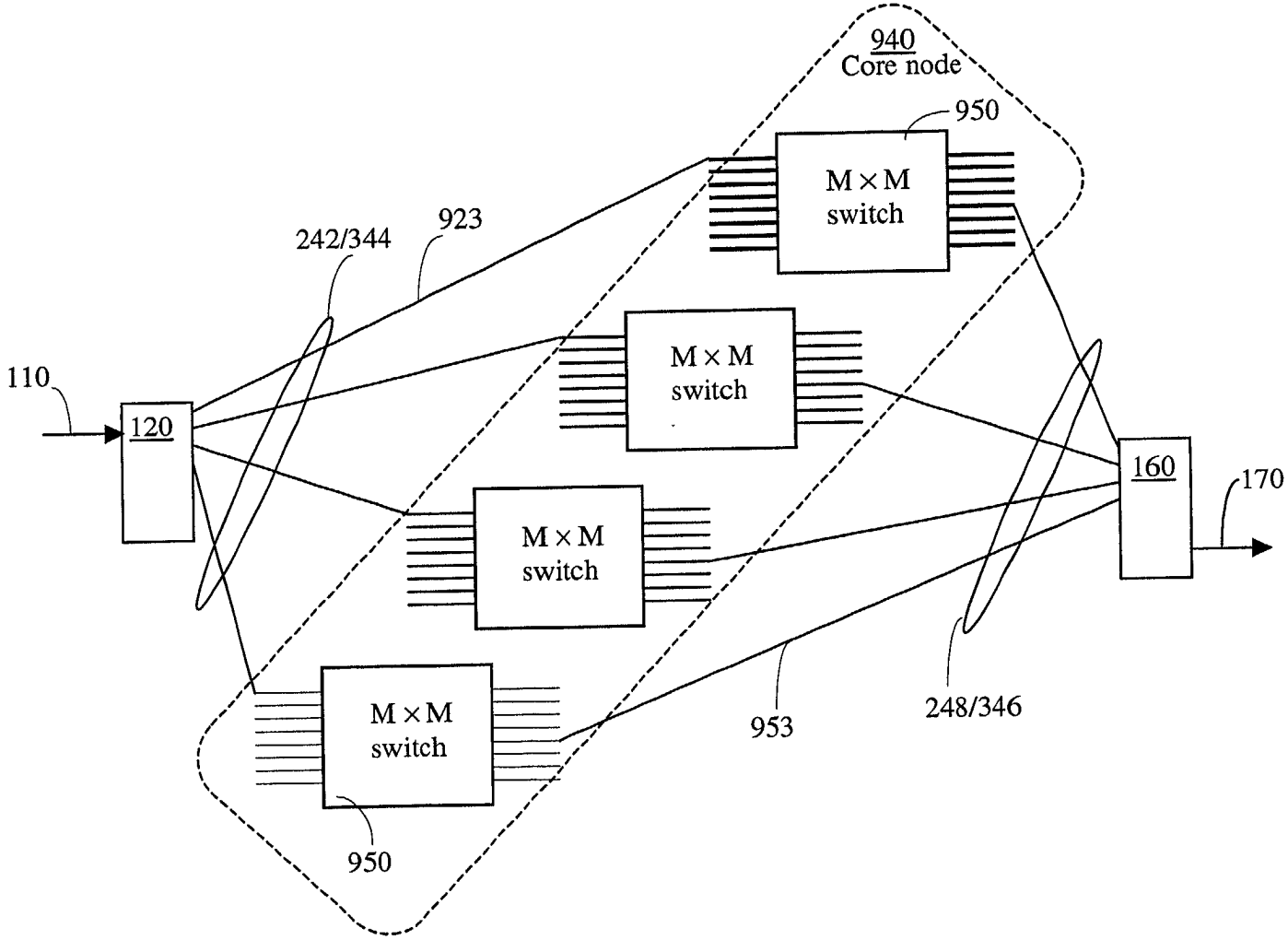

940
Core node
950
M × M
switch
242/344
923
110
120
M × M
switch
160
170
M × M
switch
M × M
switch
953
248/346
950

Fig. 9

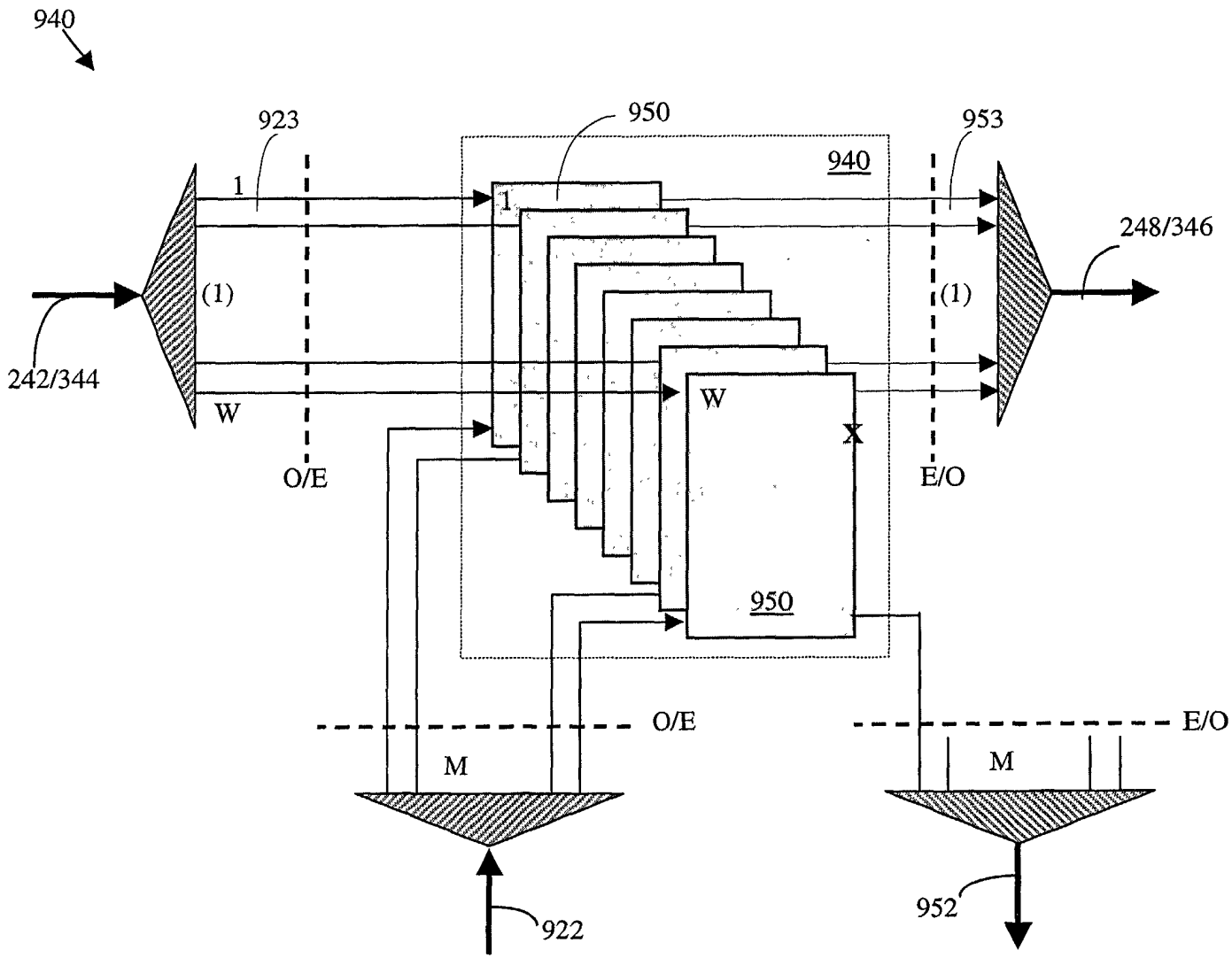

940
923
950
953
940
1
1
248/346
(1)
(1)
242/344
W
W
X
O/E
E/O
950
O/E
E/O
M
M
922
952

Fig. 10

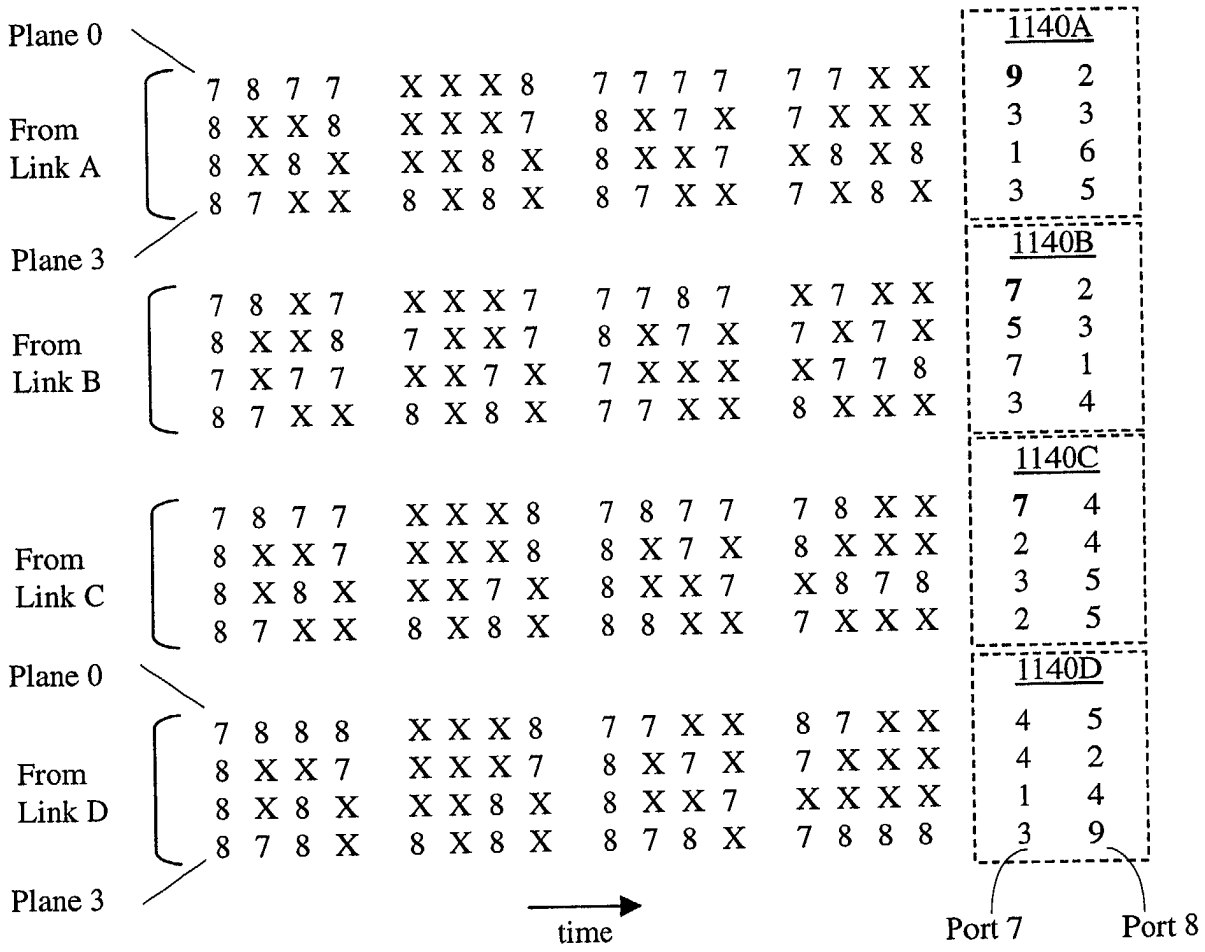

Plane 0
From Link A
Plane 3
From Link B
From Link C
Plane 0
From Link D
Plane 3
time
1140A
1140B
1140C
1140D
Port 7
Port 8

Fig. 11a

1160

	Port 7	Port 8
Link-A	16	16
Link-B	22	10
Link-C	14	18
Link-D	12	20
	64	64

Fig. 11b

1180

	Port 7	Port 8
Plane-0	27	13
Plane-1	14	12
Plane-2	12	16
Plane-3	11	23
	64	64

Fig. 11c

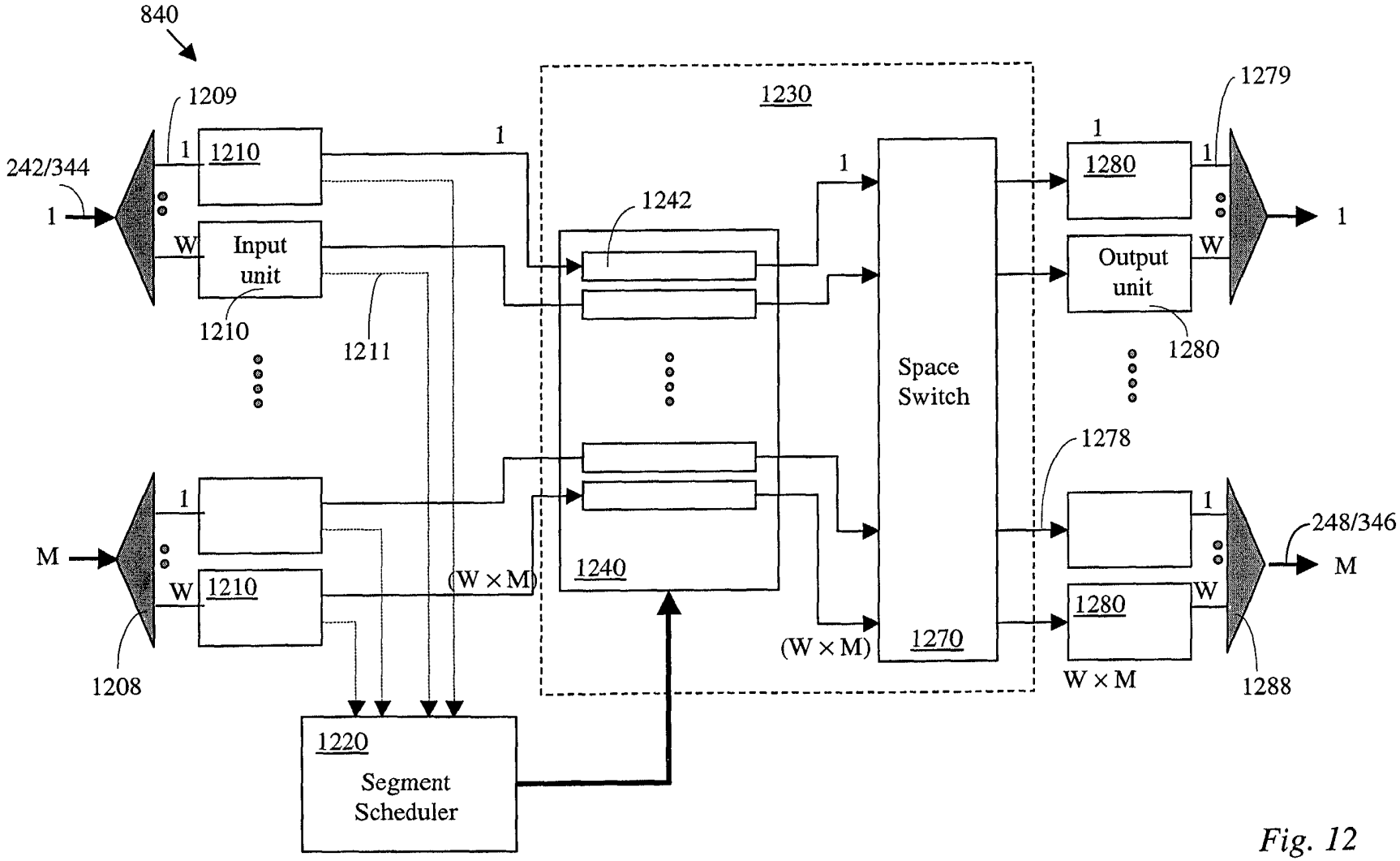

840
1209
1230
1279
242/344
1
1210
1
1
1
1280
1
1
W
Input unit
1242
Output unit
W
1
1210
1211
1280
Space Switch
1278
1
1
M
1210
W
(W × M)
1240
248/346
M
W
1280
(W × M)
1270
W × M
1208
1288
1220
Segment Scheduler

Fig. 12

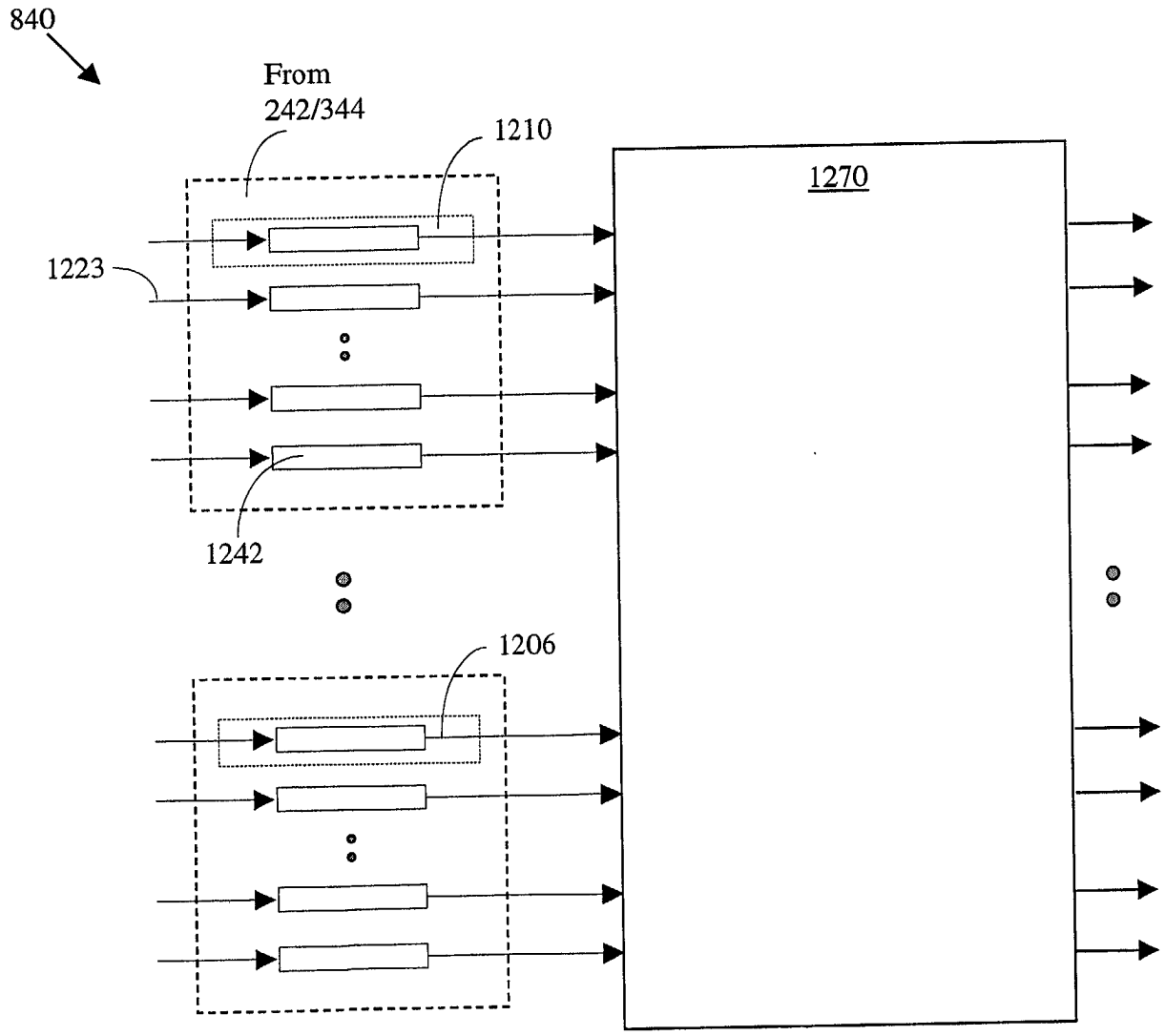


Fig. 13

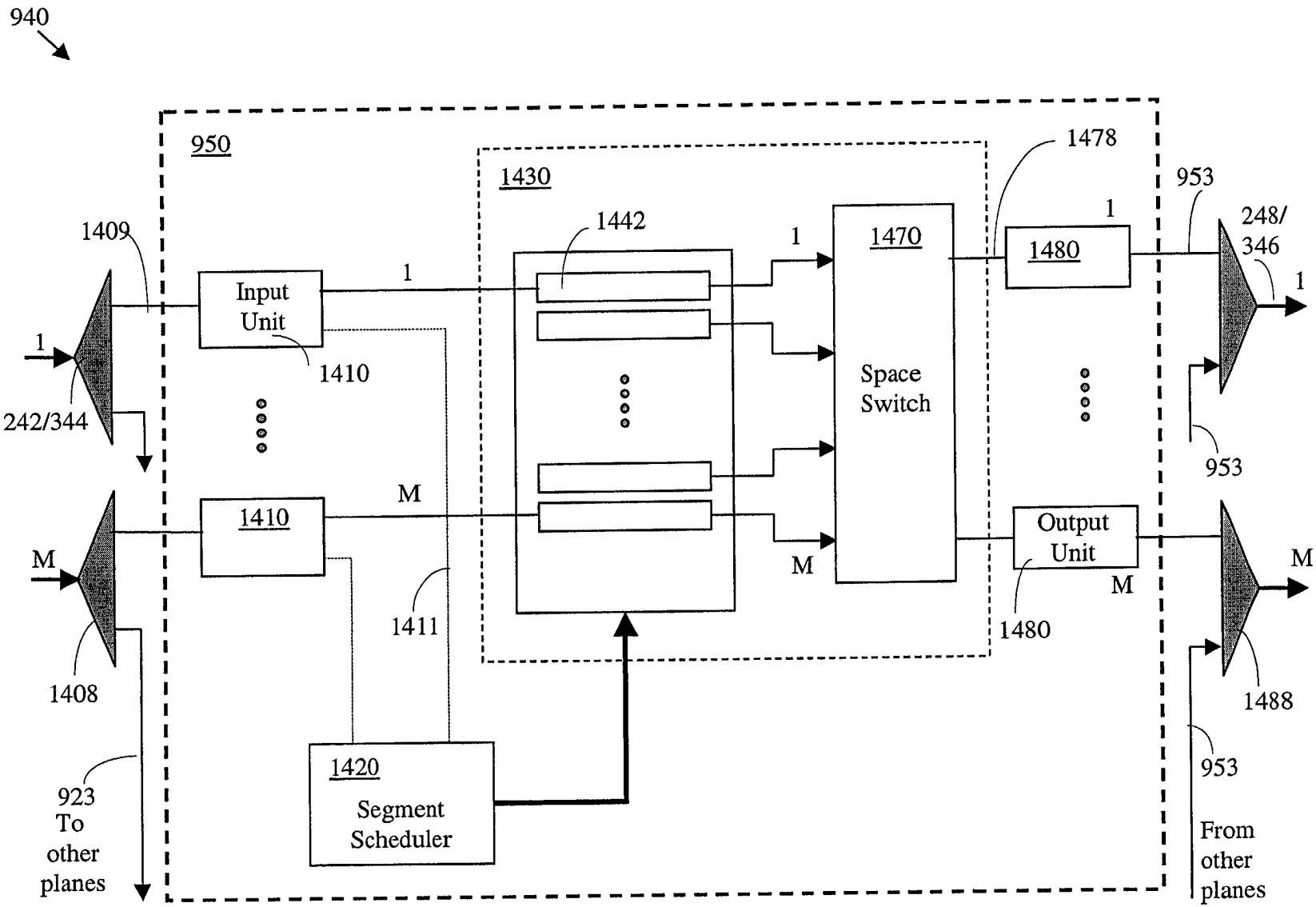

940
950
1430
1478
953
1409
1442
1
1470
1480
248/
346
Input
Unit
1
1
Space
Switch
1410
242/344
953
M
1410
Output
Unit
M
M
M
1411
1480
1408
1488
1420
Segment
Scheduler
923
To
other
planes
953
From
other
planes

Fig. 14

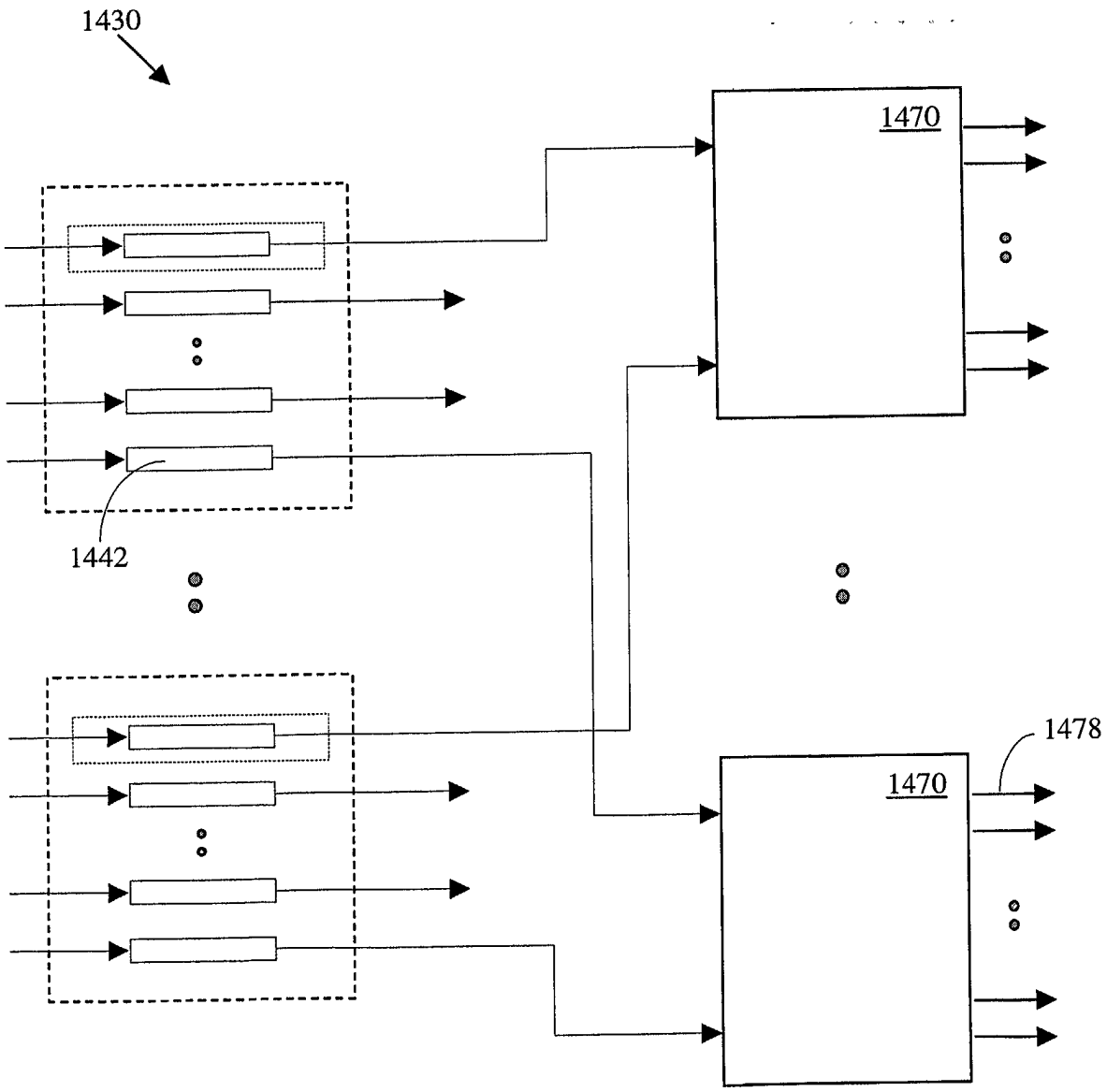


Fig. 15

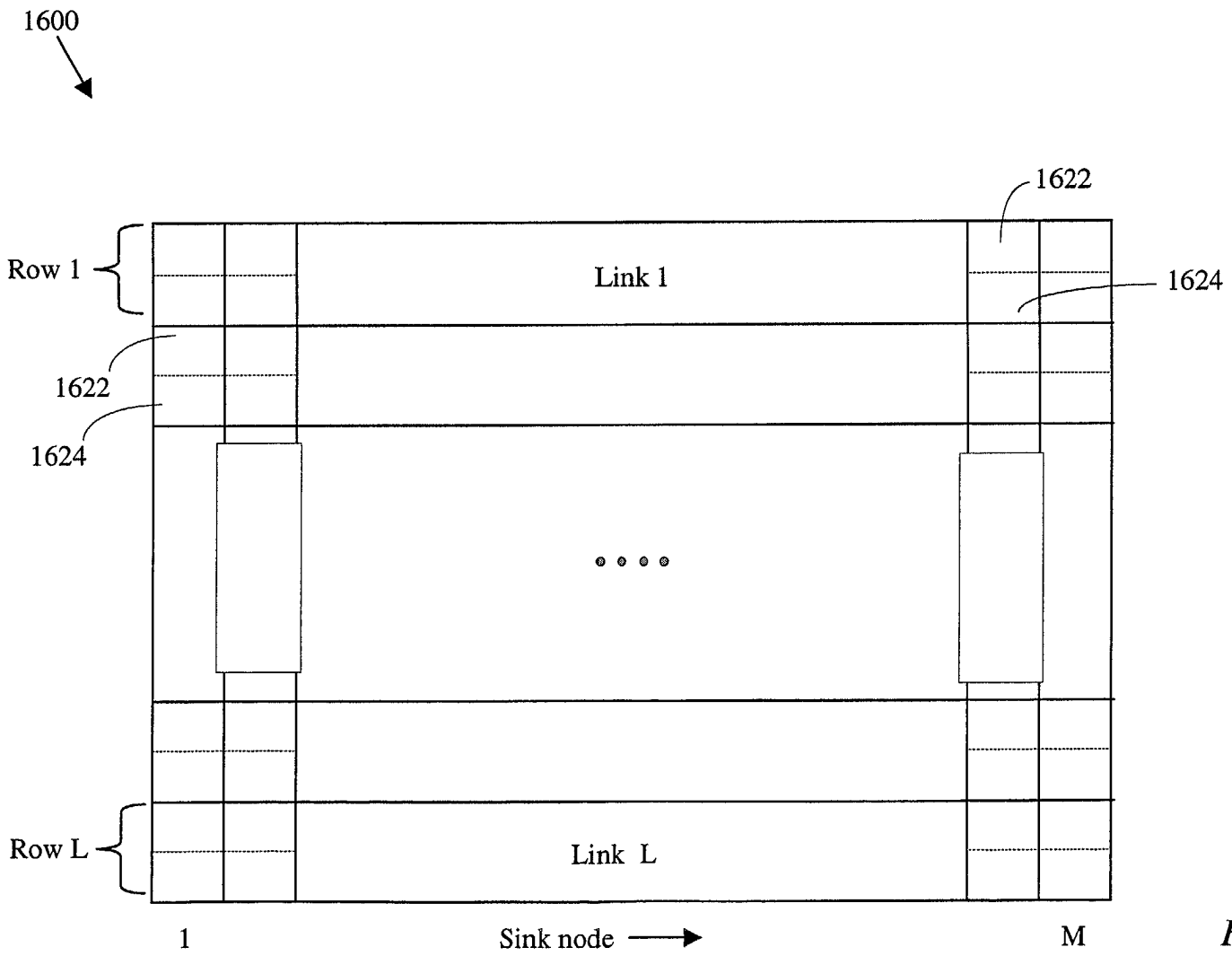


Fig. 16

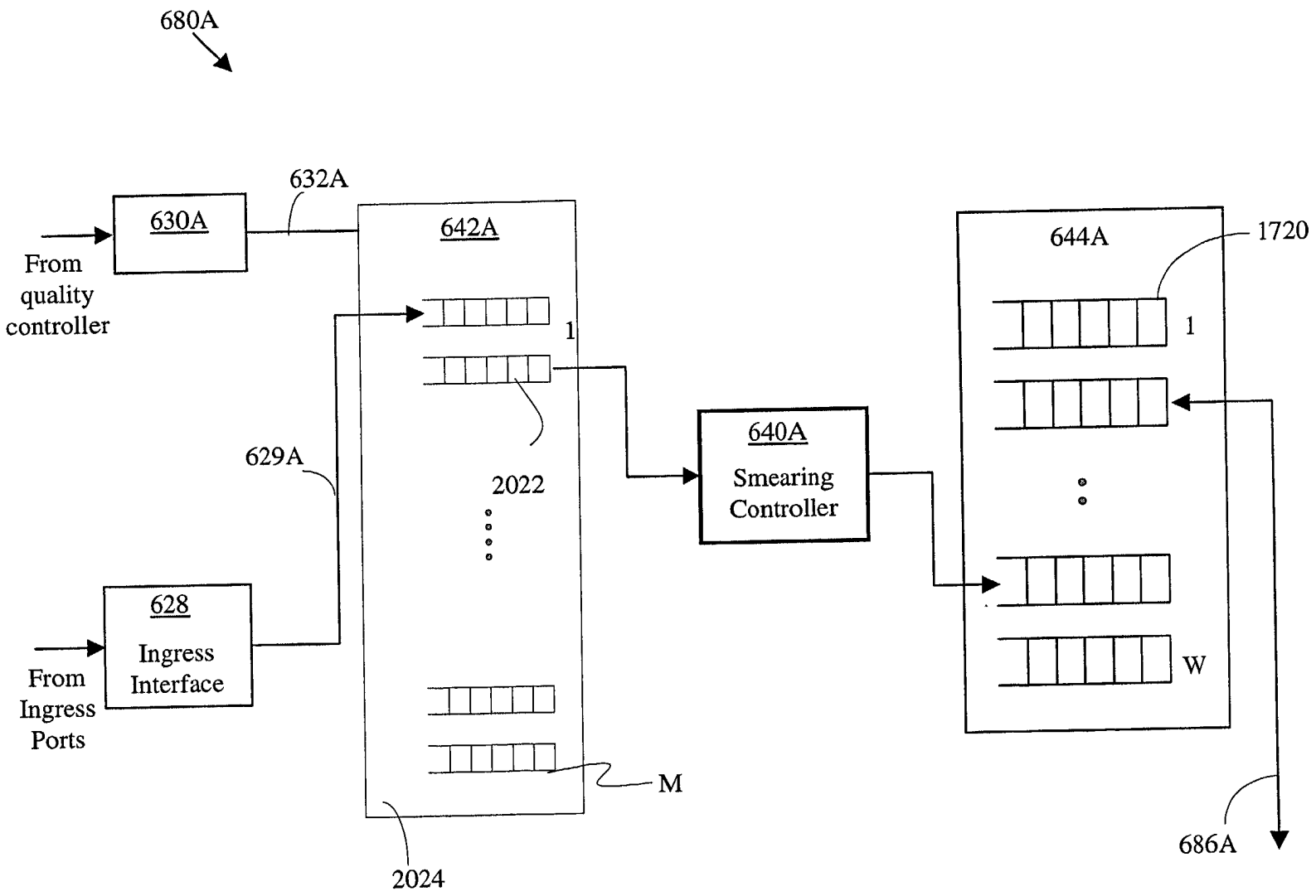

680A
632A
630A
From quality controller
642A
644A
1720
1
1
629A
2022
640A
Smearing Controller
628
Ingress Interface
From Ingress Ports
W
M
686A
2024

Fig. 17

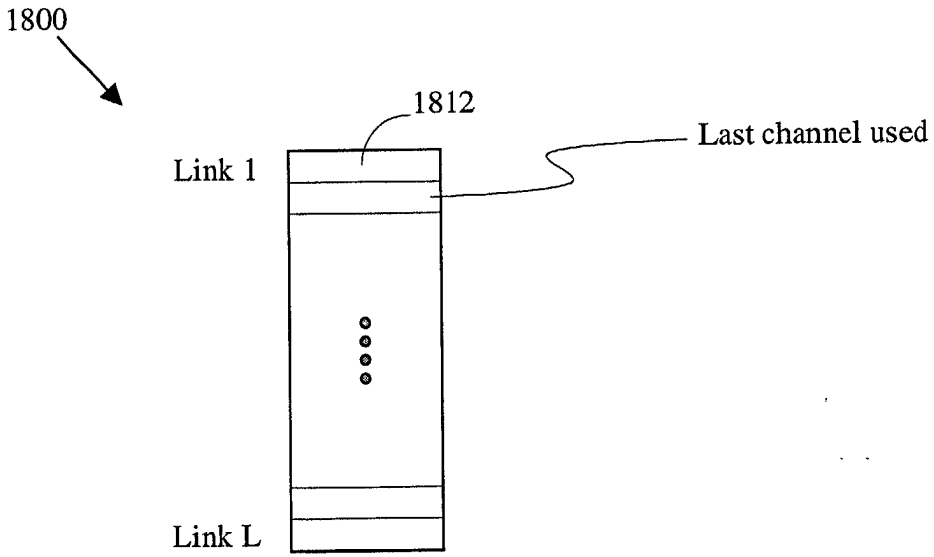


Fig. 18

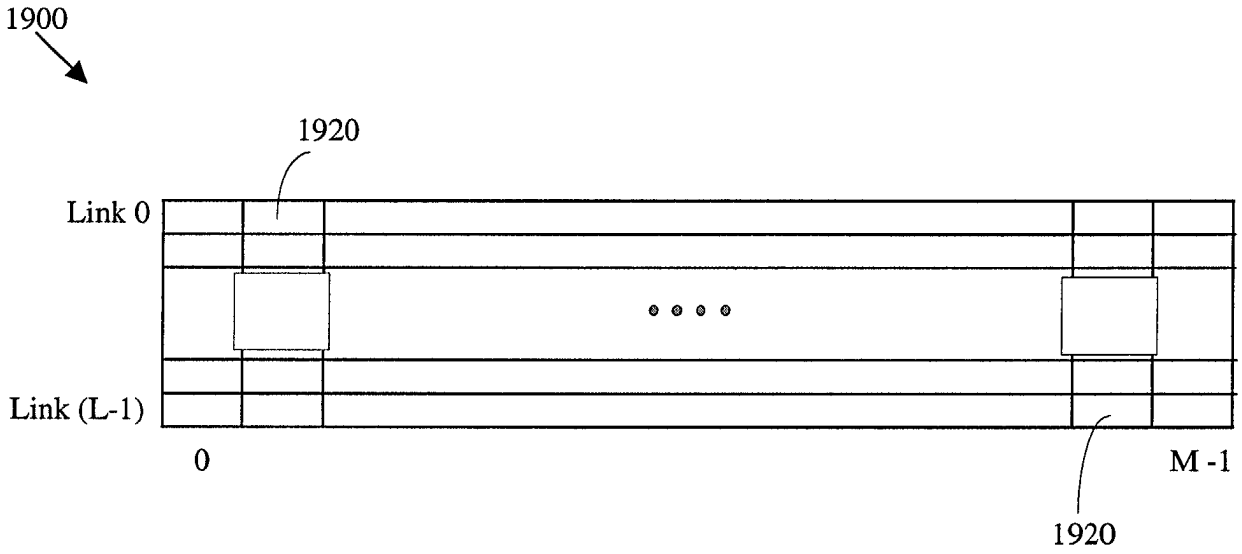


Fig. 19